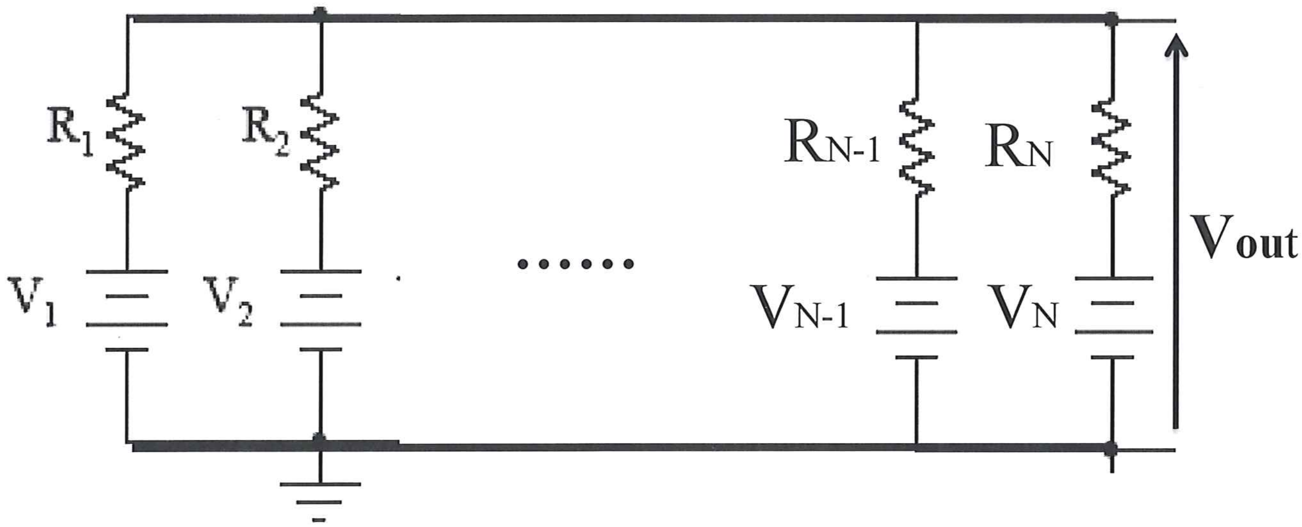
Problem 1 (2 points)

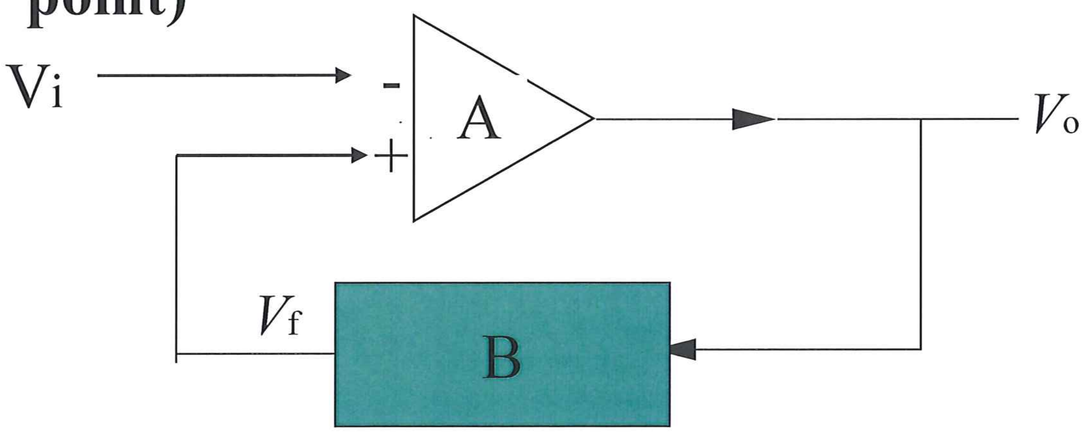
(a: 1 point)



Prove that:

$$V_{out} = \left(\sum_{i=1}^{N} \frac{V_i}{R_i}\right) / \left(\sum_{i=1}^{N} \frac{1}{R_i}\right)$$

(b: 1 point)

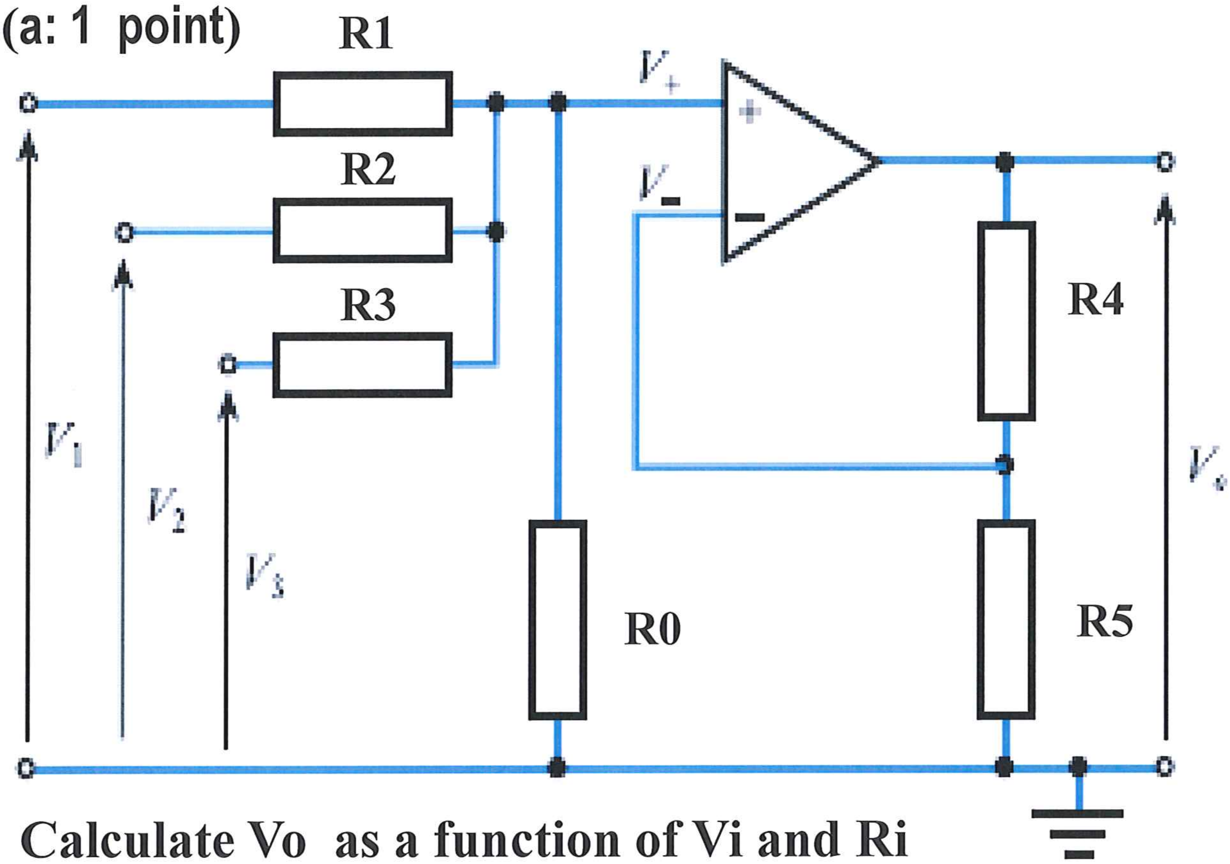


Calculate the loop gain G=Vo/Vi and indicate the condition for possible oscillation

Problem 2 (2 points)

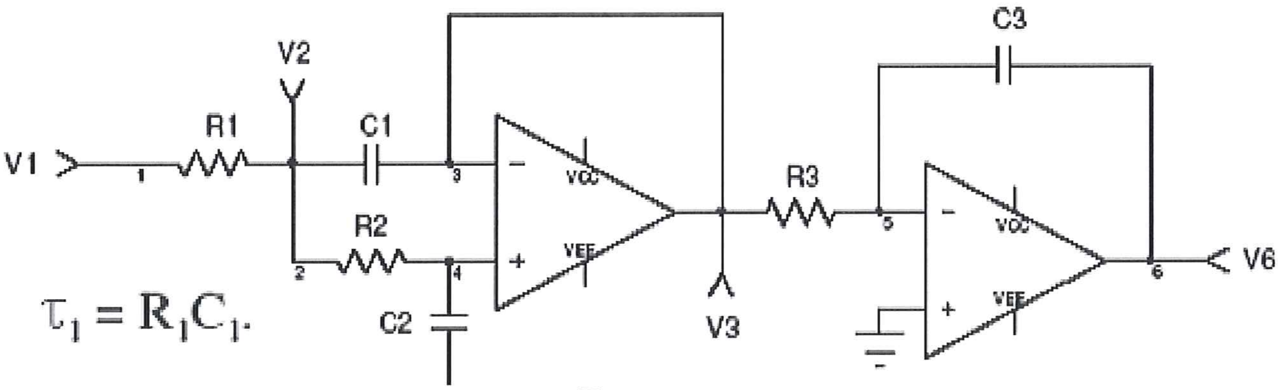
V+=V-

(a: 1 point)



Calculate Vo as a function of Vi and Ri

(b:1 point)

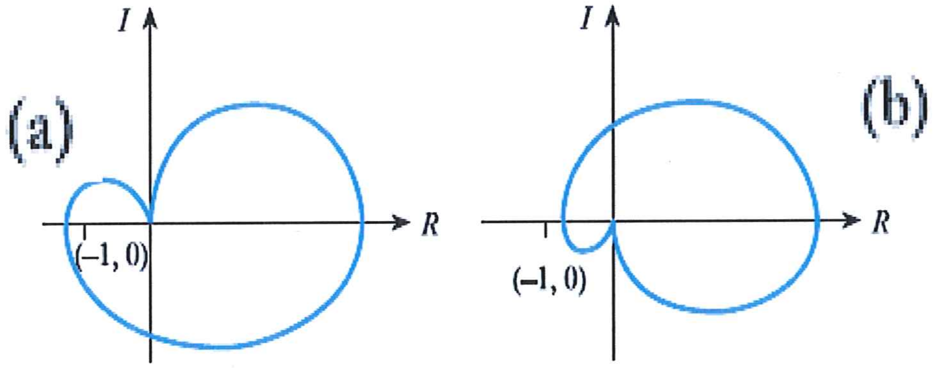


$\tau_1 = R_1 C_1.$

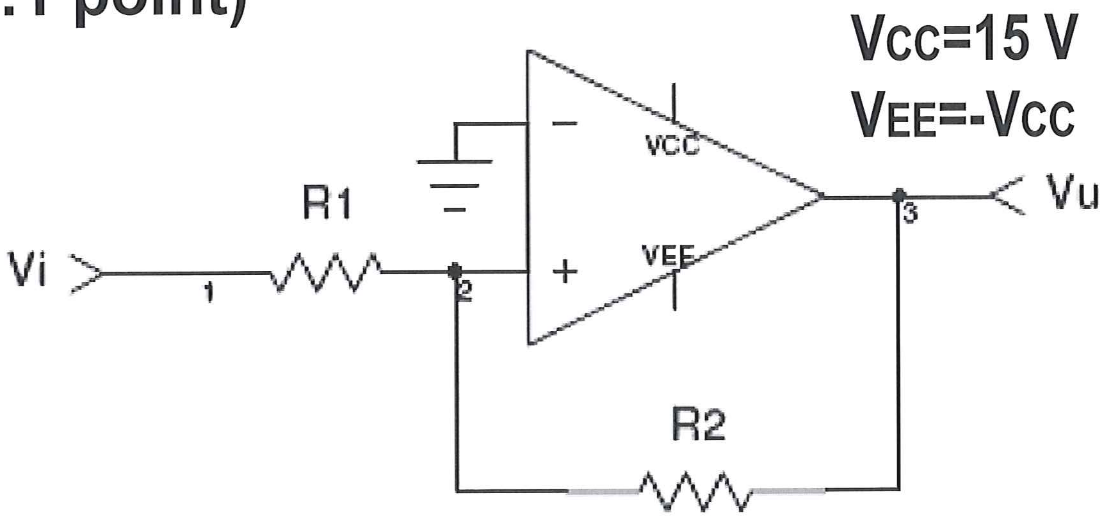
Prove that: $$V(2) = \frac{\left(\frac{R_1}{R_2} + j\omega\tau_1\right) V(3) + V(1)}{1 + \frac{R_1}{R_2} + j\omega\tau_1}$$

Problem 3 (1.5 points)

(a: 0.5 point) -The Nyquist diagrams below represent two circuits. Determine the number of low-frequency and high-frequency cut-offs and indicate which system is stable



(b:1 point)



Assume that R1=3 KΩ, R2=15 KΩ input potential
Vi= Voi sin(ωt), Voi= 5 V

→ **Draw the output potential Vu:**

Problem 4 (2 points)

(a: 1 point)

	Q3 (Before)	Q2 (Before)	Q1 (Before)	Q3 (After)	Q2 (After)	Q1 (After)
1						
2						
3						
4						

Build a synchronous 4-counter (1→4)

J	K	Q_n
0	0	Q_{n-1}
0	1	0
1	0	1
1	1	$\overline{Q_{n-1}}$

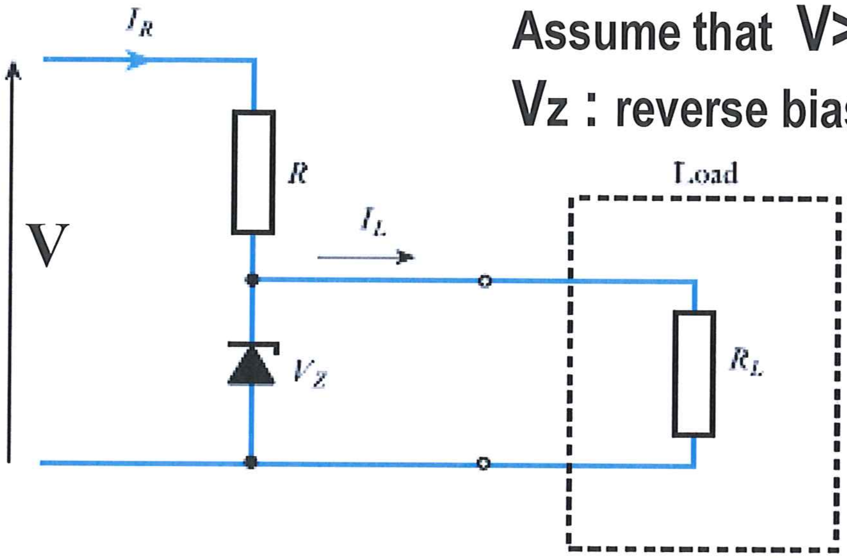
Q_{n-1}	Q_n	J	K
0	0	0	*
0	1	1	*
1	0	*	1
1	1	*	0

*: don't care

(b: 1 point)

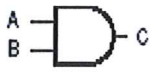
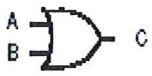
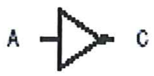
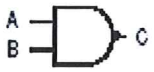
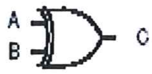
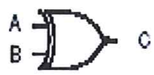
Assume that $V > V_Z$

V_Z : reverse bias voltage



For what value of R the zener diode can not conduct current under reverse bias conditions ?

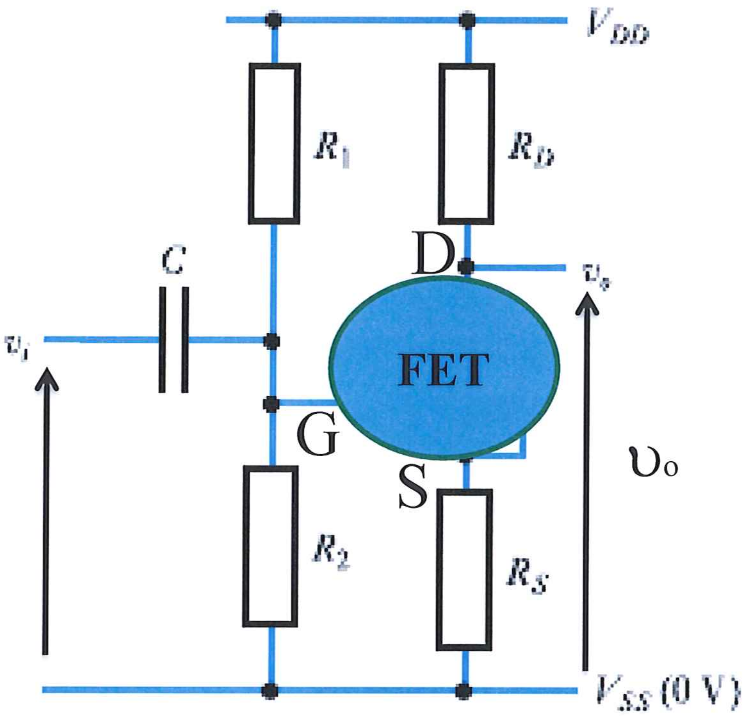
Tabel 1 Logische poorten.

Functie	Symbool	Boolean	Waarheidstabel
AND		$C = A \cdot B$	A B C 0 0 0 0 1 0 1 0 0 1 1 1
OR		$C = A \times B$	A B C 0 0 0 0 1 1 1 0 1 1 1 1
NOT		$B = \overline{A}$	A B 0 1 1 0
NAND		$C = \overline{A \cdot B}$	A B C 0 0 1 0 1 1 1 0 1
NOR		$C = \overline{A \times B}$	A B C 0 0 1 0 1 0 1 0 0 1 1 0
XOR		$C = A \oplus B$	A B C 0 0 0 0 1 1 1 0 1 1 1 0
XNOR		$C = \overline{A \ominus B}$	A B C 0 0 1 0 1 0 1 0 0

Problem 5 (2.5 points)

(a) (1 point):

If an application of a small varying input signal υ_i leads to small variation of the gate, drain, and source potentials :



$$V'_G = V_G + \upsilon_g$$

$$V'_D = V_D + \upsilon_d$$

$$V'_S = V_S + \upsilon_s$$

$$\upsilon_i = \upsilon_g, \quad \upsilon_o = \upsilon_d$$

Then show that the current I_D through the FET changes up to first order terms as:

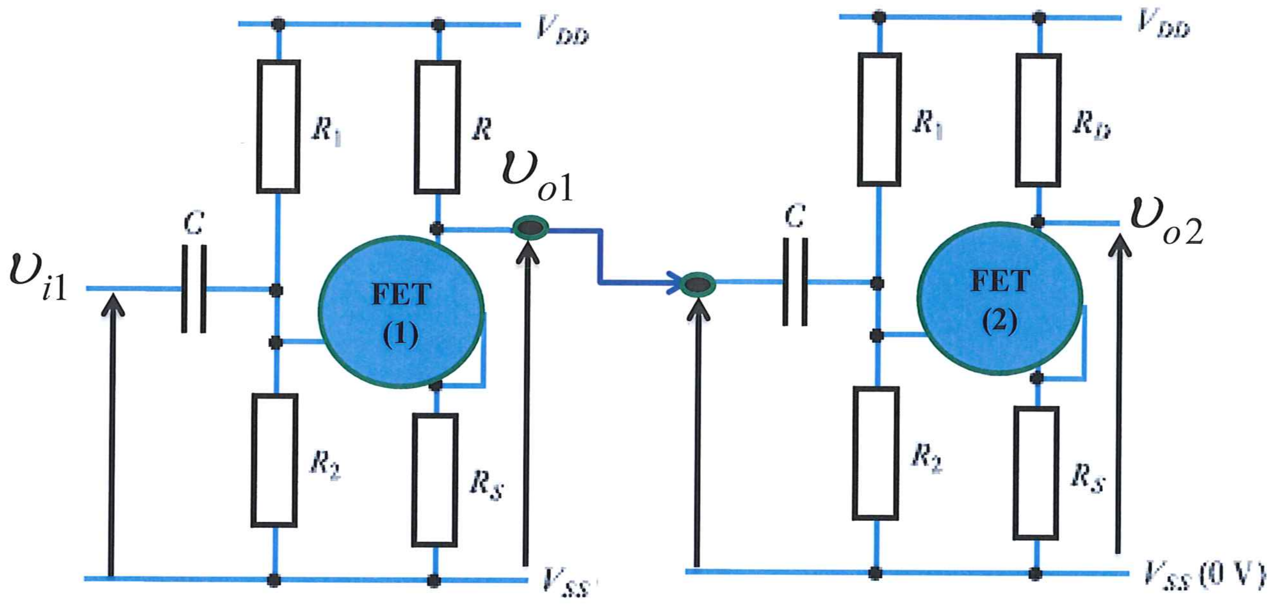
$$I'_D \approx I_D + \left\{ g_m \upsilon_{gs} + \frac{\upsilon_{ds}}{r_d} \right\} + \ldots.$$

$$I_D = I_D(V_{GS}, V_{DS})$$

$$g_m = \frac{\partial I_D}{\partial V_{GS}}, \quad 1/r_d = \frac{\partial I_D}{\partial V_{DS}} \qquad \upsilon_{gs} = \upsilon_g - \upsilon_s, \; \upsilon_{ds} = \upsilon_d - \upsilon_s$$

(b) FET amplifier (1.5 points)

Consider a cascade of two FETS in series where the output of FET(1) is the input at the gate for FET (2) :



Show that the total amplification ratio is given by (1 point):

$$\frac{\upsilon_{o2}}{\upsilon_{i1}} = \left\{ \frac{g_m R_D}{1 + g_m R_S + [(R_D + R_S)/r_d]} \right\}^2$$

For $R_{D,S} << r_d$, and $g_m R_S >> 1$ derive a simpler expression for $\upsilon_{o2}/\upsilon_{i1}$ (0.5 points)

Tip: For (b) use the knowledge from (a) or make directly the "small signal circuits of the FETs in series to compute the amplification ratio "